MICHAEL R. GALPIN
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Strong, diverse background in Electrical Engineer with extensive experience in verification, programming and digital hardware design at Motorola, AMD, IBM, Intel, and other Fortune 500 companies, leveraging analytical and problem solving skills to achieve positive results. Proficient in hardware design and programming as well as testing, simulation, verification, and debugging problems. Expertise in 80x86, ARM, and Power PC microprocessors. Experienced with Verilog, ModelSim, System Verilog, Debussy, and C++.

EMPLOYMENT HISTORY

Design Verification Engineer (contract), Qualcomm, Raleigh, NC June to Oct. 2008

- Debugged failing System Verilog verification and random tests on an ARM Architecture Verilog project, meeting testing schedules and enabling production of parts.
- Developed ARM Assembly and System Verilog tests on the ARM Architecture Snapdragon ASIC project.
- Contract position ended due to economic reasons just before successful tapeout.

Electrical Validation/Design Engineer (contract), Freescale, Austin, TX Sept. to Dec. 2007

- Run tests to characterize timing and voltage specifications, and to verify and debug SoC cores and platform IP on various Power Architecture ASIC SoC projects, meeting testing schedules and enabling production of parts.
- Created Perl script used to run tests on the Power Architecture S0C projects.
- Contract position ended at successful completion of project.

Pre-Silicon Validation Engineer (contract), Intel, Chandler, AZ. 2004 to 2005

- Adapted tests and environment, simulated, and debugged verification tests for the

Tavor three processor cell phone/PDA ASIC, enabling scheduled production of parts.

- Debugged test and environment problems using the ModelSim simulator and Debussy debugger for the Verilog HDL Project, finding many environment problems and verifying fixes.

- Updated a random test generator written in Object Oriented Perl, used to generate tests for the Tavor three processor System, removing global variables and improving code modules.

- Contract position ended after successful tapeout.

Design and Verification Engineer, ESS Technology, Austin, TX. 2000 to 2003

- Adapted tests and environment, simulated, and debugged verification tests for the Jedi north bridge Verilog HDL ASIC project. Ran logical equivalence checker to compare rtl, gates, and cadence net lists. Debugged hardware problems and wrote tests to duplicate bugs and verify fixes, fixing numerous problems and moving to next phase of project.

- Ran logical equivalence checker and simulations to verify equivalence, timing, and design problems on the ES3898 and ES3727 DVD/VCD mpeg decoders, enabling production of parts.

- Ran verification tests and debugged simulations, ran Geotest tester to screen parts for failures, debugged system boards, and put together documentation for the Mustang south bridge ASIC project, enabling project to move to next phase.

- Position eliminated after closing of Austin office.

Verification Engineer, Motorola, Austin, TX. 1997 to 2000

- Developed, simulated, and debugged assembly language verification tests for the MPC 8240 embedded system ASIC based on a Power PC processor, with main responsibility simulating and debugging system design problems. Enabling production of a series of SoC parts.

- Developed, simulated, and debugged assembly language verification tests for the MPC 107 ASIC chipset for a Power PC processor, with main responsibility simulating and debugging system design problems, enabling production of parts.

- Debugged and simulated assembly language verification tests, and updated a random test generator built with C++ for the VeComp SIMD DSP processor, with main responsibility debugging processor design problems, enabling production of test

chips.

Product Development Engineer, AMD, Austin, TX. 1995 to 1997

- Debugged and simulated x86 assembly language verification tests for the K7 processor, with main responsibility debugging processor design problems, finding several problems and verifying fixes.

- Developed and simulated x86 assembly language verification tests for the K5 and K6 processors, with emphasis on snoops and external processor interrupts, enabling production of processors.

Digital Design Engineer, IBM, Poughkeepsie, NY. 1988 to 1994

- Chip designer and developer from high level description to gate level implementation for five chips in the Central Processor on the high performance ES/9000 computer, using tools such as synthesis, logic verification, timing, and self test, delivering chips on schedule.

- Screened test floor and field problems for high performance mainframe computers. Responsible for resolving problems, implementing solutions, and managing and presenting team status. Resolved several critical customer issues that saved major accounts. Received an Excellence Team award for work on debugging field and test floor problems on the ES/9000 9021 model.

- Central Processor Recovery coordinator for high performance mainframe computers. Implemented and designed new functions and algorithms as well as problem determination of test floor problems, and designed fixes involving hardware, microcode, and 31 processor controller code modules. Received an award for debugging problems on the ES/9000 9021 Processor Availability Feature.

Geophysicist, Denver, CO. and Bartlesville, OK. 1974 to 1986

- Worked for three major oil companies interpreting seismic geophysical data, supervising field crews, and computer processing and computer mapping of seismic data. Discovered oil fields in North Dakota.

EDUCATION

B.S., Electrical Engineering, University of Colorado, Denver, Colorado, 1988

B.S., Geological Engineering, University of Missouri at Rolla, Rolla, Missouri, 1974